Amendments to the Drawings

Please replace existing Figure 8 and Figure 10 with Figure 8 and Figure 10 in the attached replacement sheets.

Attachment: Replacement Sheet(s) 11 and 13

REMARKS

Claims 1-45 are pending.

Summary of Telephonic Interview

The undersigned wishes to thank Examiner Kawsar for taking the time to conduct a telephonic interview on April 17, 2008. During the interview the discussion focused on the differences between the applicant's invention and the cited reference Wilt. Proposed amendments to the claims to better clarify these references were sent to the Examiner for review to which the Examiner responded favorably. The Examiner indicated that in addition to the proposed amendments, more clarity as to the paging buffer would aid in moving the application forward. The proposed amendments were modified to include this clarity.

Claim Amendments

While the applicants disagree with the basis for certain rejections made in the Official Action, claims 1, 7, 15, 16, 18-21, 23, 24, 32, 37 and 38 are nonetheless amended to expedite prosecution. Claim 17 is cancelled and claim 46 is added. No new matter has been added due to these amendments and support for these amendments can be found throughout the applicant's specification and figures.

Objection to Specification

The Office has objected to the specification because "on page 14 paragraph 37 and 38 should be one paragraph."

The applicants submit herewith the replacement paragraph listed hereinbefore.

Objection to Drawings

The Office has objected to the drawings "because fig. 8 and 10 have shaded portion that are not clear after scanning" and requires corrected drawing sheets in compliance with 37 CFR 1.121(d).

Accordingly, the applicants submit herewith replacement sheets for Figure 8 and Figure 10 in compliance with 37 CFR 1.121(d).

Objection to Information Disclosure Statement

The Office has objected to the information disclosure statement because it "fails to comply with 37 CFR 1.98(a)(2)." Applicants acknowledge the objection, and will submit a supplemental IDS in compliance with 37 CFR 1.98(a)(2) including legible copies of cited documents.

Claim Rejections under 35 U.S.C. §101

Claims 15-31 stand rejected under 35 U.S.C. 101 "because the claimed invention is directed to non-statutory subject matter."

The applicants submit that claim 15 is amended to recite a statutory computer readable storage medium as suggested in the Official Action. Claims16 and 17 are canceled. Independent claim 18 is amended to explicitly recite a coprocessor, thereby explicitly including a statutory hardware element in claims 18-31. Accordingly, claims 15-31 are now clearly patentable under 35 U.S.C. § 101.

Claim Rejections under 35 U.S.C. §112

Claims 1-45 stand rejected under 35 U.S.C. 112, second paragraph "as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention." Specifically, regarding claims 1, 18 and 32, the Office asserts that these claims include claim language that is unclear. Furthermore, claim 32 is rejected because it appears to be "a method claim directed to computer system/device" while "dependent claims 33-45 are directed to computer device claims."

First, with regard to item 13 of the Official Action, Applicants observe that the Examiners interpretation of claim 32 as a system/device claim is correct. Appropriate language is included in the preamble of claim 32 to correct the inconsistency.

With regard to item 12 of the Official Action, Applicants correct herewith the identified issues. In general, Applicants direct the Examiner to paragraphs 37-50 of Applicants specification. Claims 1, 18 and 32 are amended to as follows:

- The term "coprocessor resources" is removed from the claims, and the claims are clarified to recite that coprocessor operations are scheduled.

- The term "analyzing" is removed from the claims.
- The "at least one memory resource" is clarified to more specifically recite "at least one graphics data memory resource." This is not the same as the paging DMA buffer. The paging DMA buffer is a buffer with instructions to move memory resources to an assigned location so they can be efficiently processed by the coprocessor.
- The term "instructs" is removed from the claims, and language is added to clarify that the paging DMA buffer includes an instruction for the coprocessor to move a memory resource.
- The final element of the claims is recited to clarify that the content of the DMA buffer is processed.

Claim Rejections under 35 U.S.C. §102

Claims 1-25 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 7,234,144 to Wilt et al. (hereinafter "Wilt"). The Applicants respectfully disagree with these rejections and request favorable reconsideration in view of the following remarks.

Regarding the rejection of independent claims 1, 18 and 32, the Office asserts that Wilt teaches "receiving by a kernel mode driver a command buffer from a user mode driver, wherein the command buffer is formulated based on a work request submitted to the coprocessor," citing Wilt column 23, lines 62-65 and column 25, lines 29-34:

> The system described in this document can expose display list functionality readily by using the user mode driver interface that translates DDI level commands to hardware-specific commands.

and,

> The command buffer scheduler 404 ("scheduler") and kernel driver 405 work together in kernel mode to dispatch command buffers to the hardware 406 (the scheduler 404 decides which command buffer should be dispatched, while the kernel driver 405 instructs the hardware 406 to dispatch a command buffer at the request of the scheduler).

However, this language from Wilt merely discloses a user mode driver interface that translates DDI level commands to hardware-specific commands and a kernel driver that instructs the hardware to dispatch a command buffer. This is not the same or even similar to that claimed by the applicants. And in fact, this is in contradiction to the applicant's

invention which claims a kernel mode driver receiving a command buffer from a user mode driver.

Additionally, the Office asserts that Wilt discloses "generating by the kernel mode driver at least one direct memory access (DMA) buffer based on said command buffer and a resource list corresponding to at least one memory resource associated with processing said at least one DMA buffer by said coprocessor, wherein a set of at least one DMA buffer is maintained for each client context" and directs the applicant's attention to column 25, lines 10-14 and column 24, lines 57-61 of Wilt:

> FIG. 4 depicts an exemplary user mode driver DLL implementation of the above-described invention. In FIG. 4, the application 401, runtime 402 and part of the driver 404 operate in user mode to write drawing commands into hardware-specific command buffers in DMA memory.

and,

> In the context of this invention, GPU resources such as video memory similarly can be virtualized by tracking the resources needed for execution of a given command buffer and ensuring that those resources are available when the command buffer is issued to the hardware.

These sections of Wilt disclose an "exemplary user mode driver DLL implementation" where the user mode driver writes "drawing commands into hardware-specific command buffers in DMA memory," and virtualizing GPU resources by "tracking the resources needed for execution of a given command buffer." This is not the same or even similar to that claimed by the applicants. In fact, the applicant's claim is directed to a kernel mode driver and not a user mode driver. This is important in that they are separate and distinct elements. For example, a user mode driver can only access specific applications resources, while the kernel mode driver has access to the system resources. Accordingly, when a kernel mode driver fails, the entire system typically crashes, whereas when a user mode driver fails, only the current process typically crashes. Additionally, Wilt does not teach or disclose a resource list, let alone a resource list corresponding to at least one memory resource which is associated with processing the DMA buffer. Lastly, in the cited passages, Wilt does not disclose maintaining a set of DMA buffers for each client context.

For these reasons, the applicants respectfully submit that independent claims 1, 18 and 32 are clearly not anticipated and thus patentable over Wilt. And claims 2-16, 19-31 and 33-

45, which depend therefrom respectively, are also not anticipated and thus patentable over Wilt for the same reasons. Nevertheless, the applicants wish to point out the following additional reasons why certain dependent claims are not anticipated and thus patentable over Wilt.

Regarding the rejection of claim 4, the Office asserts that Wilt discloses submitting the paging buffer to the coprocessor and directs the applicant's attention to column 18, lines 4-6 as support. The applicants disagree and assert that the cited passages of Wilt merely disclose a command buffer entering steady state and a scheduler considering the command buffer for submission to the coprocessor. This is clearly not the same as that claimed by the applicant as a command buffer is not the same as a paging buffer. The applicant's specification makes this clear by defining a "command buffer" as "a buffer built by the user mode driver and is regular pageable memory allocated in the context of the rendering application (see paragraph [0055]) and a "paging buffer" as "a buffer built by the kernel mode driver to page in/evict/ move memory resources needed for a particular DMA buffer (see paragraph [0058]).

Regarding the rejection of claim 5, the Office asserts that Wilt discloses assigning priority to elements in the DMA buffer and directs the applicant's attention to column 18, lines 8-11 as support. The applicants disagree and assert that the cited passages of Wilt merely disclose that from a plurality of buffers, prioritizing the submission of the buffers. Wilt makes no mention, suggestion or teaching of prioritizing the contents of the buffer. This is clear from the cited passage in Wilt which recites in part,

> The scheduler has a great deal of flexibility in deciding ***which command buffer should be submitted*** to the hardware. The scheduler may take into account ***the priority***, if any, ***of the command buffer***, the priority of the requesting thread, ...

Clearly, Wilt does not disclose the elements of claim 5.

Regarding the rejection of claim 6, the Office asserts that Wilt discloses that the paging buffer includes at least one command that requests the coprocessor to stop processing and directs the applicant's attention to column 29, lines 17-29 as support. The applicants disagree and assert that the cited passages of Wilt merely disclose that if a GPU context is affiliated with a CPU thread, suspending that thread makes the GPU context unavailable until

the CPU thread is unblocked. This is clearly not the same or even similar to that claimed in claim 6.

Regarding the rejection of claim 9, the Office asserts that Wilt discloses a coprocessor that processes the DMA buffer in a different order that the order in which the DMA buffer is generated and directs the applicant's attention to column 25, lines 4-9 as support. The applicants disagree and assert that the cited passages of Wilt merely disclose that the operating system has to keep track of and 'fix up' references to video memory surfaces before dispatching the command buffer to the hardware. Wilt makes no reference or mention of a coprocessor that processes the DMA buffer in a different order that the order in which the DMA buffer was generated.

Regarding the rejection of claim 10, the Office asserts that Wilt that the coprocessor is busy processing another DMA buffer during at least one of receiving, generating, analyzing and submitting and directs the applicant's attention to column 19, lines 30-33 as support. The applicants disagree and assert that the cited passages of Wilt merely states that "interrupts may be used for efficient management of coprocessors' computational resources." Wilt does not disclose processing another DMA buffer during at least one of receiving, generating, analyzing and submitting as claimed.

Regarding the rejection of claim 11, the Office asserts that Wilt interrupting the processing of a DMA buffer and resuming the processing of the interrupted DMA buffer and directs the applicant's attention to column 19, lines 41-50 as support. The applicants disagree and assert that the cited passages of Wilt merely disclose that "when a command buffer is finished executing, the system is notified so it can select another command buffer to submit to the hardware." Wilt does not disclose interrupting the processing of the DMA buffer and resuming processing of the interrupted DMA buffer as claimed.

Regarding the rejection of claims 12 and 13, the Office asserts that Wilt discloses determining whether the DMA buffer implicates a threshold amount of memory resources and directs the applicant's attention to column 24, lines 4-14 as support. The applicants disagree and assert that the cited passages of Wilt merely disclose the translation of the commands' DDI counterparts, writing them to temporary buffers and then allocating command buffers of suitable sizes. This is not the same as determining whether the DMA

buffer implicates a threshold amount of memory resources and then if the DMA buffer implicates more than the threshold amount, splitting the DMA buffer.

Accordingly, in light of the above it is very clear that Wilt does not disclose or teach the elements of claims 1-45 and thus, these claims are clearly patentable over Wilt. Accordingly, the applicants respectfully requests that the Office favorably reconsider and withdraw these rejections.

CONCLUSION

For all the foregoing reasons, the Applicants respectfully submit that the present application is now in condition for allowance.

Date: April 25, 2008

/Nathaniel Gilder/
Nathaniel Gilder
Registration No. 53,233

Woodcock Washburn LLP
Cira Centre
2929 Arch Street, 12th Floor
Philadelphia, PA 19104-2891
Telephone: (215) 568-3100
Facsimile: (215) 568-3439